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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,547	07/16/2003	Sung-Hee Cho	SAM-0479	8430
7590 12/20/2004			EXAMINER PATEL, RAJNIKANT B	
Anthony P. Onello, Jr. MILLS & ONELLO LLP Suite 605 Eleven Beacon Street Boston, MA 02108			ART UNIT 2838	
DATE MAILED: 12/20/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/620,547

Applicant(s)

CHO, SUNG-HEE

Examiner

Rajnikant B Patel

Art Unit

2838

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 July 2003.
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-6 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 7/28/04.

- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Murari et al. (U.S. Patent # 5,036,269).

Murari et al. Discloses claimed invention an internal voltage generation circuit (figure 1-3), including a voltage divider (figure 1, item R1 and R2), a comparator (figure 1, item A), a reference voltage (figure 1, item VR) and a driver for supplying the external voltage (figure 1, item OUT).

3. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Jeon (U.S. Patent # 5,747,974).

Jeon discloses claimed invention an internal voltage generation circuit (figures 1,3 and 5), including a voltage divider, a comparator (figure 3, item 13a), a serially connected resistors (figure 3, item 15a), a reference voltage generator (figure 3, item 12).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's prior art figure 3 in combinations with Bertails et al. (U.S. Patent # 4,442,398).

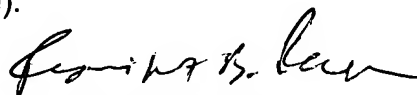
Applicant prior art disclose the claimed invention except the utilization of the technique for a first and second diode type NMOS transistor for bias current reference. However Bertails et al. teaches the similar technique for a first and second diode type NMOS transistor for bias current reference (figure 1, item 20 and 24). It would have been obvious one having an ordinary skill in the art at the time the invention was made to modify Applicant's prior art internal voltage generator circuit by utilizing the technique taught by Whatley for the purpose of improving bias current reference circuit.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rajnikant B Patel whose telephone number is 571-272-2082. The examiner can normally be reached on 6.30-5.00; m-f.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 571-272-2084. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Rajnikant B Patel
Primary Examiner
Art Unit 2838
